AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A capacitance detection circuit comprising:

a first buffer amplifier unit connected to a capacitor to be detected via a signal wire;

a first diode and a second diode connected in series between the signal wire and a first power supply; and

a third diode and a fourth diode connected in series between the signal wire and a second power supply,

wherein:

an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance;

the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and

the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor.

2. (Original) The capacitance detection circuit according to Claim 1, wherein a voltage gain of the first buffer amplifier unit is 1.

3. (Cancelled)

4. (Currently Amended) The capacitance detection circuit according to Claim 3, wherein the first resistor and the first capacitor are~~, respectively, a resistance value and a capacitance value~~ components of a high pass filter that ~~pass~~ passes frequency elements of output signals from the first buffer amplifier unit corresponding to variant capacitance of the capacitor to be detected and AC component of biased voltage added to said capacitor to be detected, and

the second resistor and the second capacitor are, respectively, a resistance value and a capacitance value that pass frequency elements of output signals from the first buffer amplifier unit corresponding to variant capacitance of the capacitor to be detected and AC component of biased voltage added to said capacitor to be detected.

5. (Original) The capacitance detection circuit according to Claim 3, further comprising:

a second buffer amplifier unit connected between (i) a junction point of the first resistor and the first capacitor and (ii) the first junction point; and

a third buffer amplifier unit connected between (i) a junction point of the second resistor and the second capacitor and (ii) the second junction point.

6. (Currently Amended) The capacitance detection circuit according to Claim 5, wherein each voltage gain of the first to third buffer amplifier units is set so that ~~potential~~ voltage of the first junction point and ~~potential~~ voltage of the second junction point are same as ~~potential~~ voltage of the signal wire.

7. (Original) The capacitance detection circuit according to Claim 1, wherein the first buffer amplifier unit includes a MOSFET as an input circuit, a gate of the MOSFET is connected to an input terminal of the first buffer amplifier unit, and a substrate of the MOSFET is connected to an output terminal of the first buffer amplifier unit.

8. (Original) The capacitance detection circuit according to Claim 1, further comprising:

a testing terminal for an input of a testing signal; and

a testing capacitor and a switch connected in series between the input terminal of the first buffer amplifier unit and the testing terminal.

9. (Currently Amended) A circuit that detects capacitance of a capacitor to be detected, comprising:

a buffer amplifier unit connected to the capacitor to be detected via a signal wire and of which voltage gain is 1;

a first diode and a second diode connected in series between the signal wire and a first power supply in a way that a current flows from the signal wire to the first power supply via the first and second diodes;

a third diode and a fourth diode connected in series between the signal wire and a second power supply in a way that a current flows from the second power supply to the signal wire via the third and fourth diodes; and

a resistor connected between the signal wire and ~~potential~~ voltage that is equal to or lower than ~~potential~~ voltage of the first power supply and equal to or higher than ~~potential~~ voltage of the second power supply,

wherein:

an output terminal of the buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance;

the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and

the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor.

10. (Currently Amended) A circuit that detects capacitance of a capacitor to be detected comprising:

a buffer amplifier unit connected to the capacitor to be detected via a signal wire and of which voltage gain is 1;

a first diode and a second diode connected in series between the signal wire and a first power supply in a way that a current flows from the signal wire to the first power supply via the first and second diodes;

a third diode and a fourth diode connected in series between the signal wire and a second power supply in a way that a current flows from the second power supply to the signal wire via the third and fourth diodes;

a resistor connected between (i) ~~potential~~ voltage that is equal to or lower than ~~potential~~ voltage of the first power supply and equal to or higher than ~~potential~~ voltage of the second power supply and (ii) the signal wire,

a capacitor connected between an output terminal of the buffer amplifier unit and a first junction point of the first diode and the second diode;

a resistor connected to the first junction point and to a point having ~~potential~~ voltage between ~~potential~~ voltage of the first power supply and ~~potential~~ voltage of the signal wire;

a capacitor connected between the output terminal of the buffer amplifier unit and a second junction point of the third diode and the fourth diode; and

a resistor connected to the second junction point and to a point having ~~potential~~ voltage between ~~potential~~ voltage of the second power supply and ~~potential~~ voltage of the signal wire.

11. (Currently Amended) A circuit that detects capacitance of a capacitor to be detected, comprising:

a first buffer amplifier unit connected to the capacitor to be detected via a signal wire and of which voltage gain is 1;

a first diode and a second diode connected in series between the signal wire and a first power supply in a way that a current flows from the signal wire to the first power supply via the first and second diodes;

a third diode and a fourth diode connected in series between the signal wire and a second power supply in a way that a current flows from the second power supply to the signal wire via the third and fourth diodes;

a first capacitor and a second buffer amplifier unit connected in series between an output terminal of the first buffer amplifier unit and a first junction point of the first diode and the second diode;

a first resistor connected to a junction point of the first capacitor and the second buffer amplifier unit and to a point having ~~potential~~ voltage between ~~potential~~ voltage of the first power supply and ~~potential~~ voltage of the signal wire;

a second capacitor and a third buffer amplifier unit connected in series between the output terminal of the first buffer amplifier unit and a second junction point of the third diode and fourth diode;

a second resistor connected to a junction point of the second capacitor and the third buffer amplifier unit and to a point having ~~potential~~ voltage between ~~potential~~ voltage of the second power supply and ~~potential~~ voltage of the signal wire; and

a third resistor connected between (i) ~~potential~~ voltage that is equal to or lower than ~~potential~~ voltage of the first power supply and equal to or higher than ~~potential~~ voltage of the second power supply and (ii) the signal wire.

12. (Original) A method that detects capacitance of a capacitor to be detected, comprising:

connecting the capacitor to be detected and a buffer amplifier unit of which voltage gain is 1 via a signal wire;

connecting a first diode and a second diode in series between the signal wire and a first power supply and connecting a third diode and a fourth diode in series between the signal wire and a second power supply; and

canceling capacitance of the first diode and the third diode connected to the signal wire by connecting an output terminal of the buffer amplifier unit to a junction point of the first diode and the second diode via a first capacitance and to a junction point of the third diode and the fourth diode via a second capacitance;

wherein the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and

the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor.

13. (New) The capacitance detection circuit according to claim 1, further comprising an AC power supply,

wherein the capacitor to be detected is connected between the signal wire and an output terminal of the AC power supply.

14. (New) The capacitance detection circuit according to claim 13, further comprising:

n first high pass filter connected between the first buffer amplifier unit and the first junction point; and

a second high pass filter connected between the first buffer amplifier unit and the second junction point,

wherein the first high pass filter and the second high pass filter pass frequency elements corresponding to an AC voltage outputted from the AC power supply and to variant capacitance of the capacitor for detection, wherein the frequency elements are included in a signal outputted from the first buffer amplifier unit.

15. (New) The capacitance detection circuit according to claim 8,

wherein the testing capacitor, the switch, and the first buffer amplifier unit are connected so that the testing capacitor can be connected, via the switch, between the input terminal and an output terminal of the first buffer amplifier unit.